CLAIMS

What is claimed is:

1. A method of fabricating a silicide on the surface of a SiGe containing substrate comprising the steps of:

providing a structure including a Co layer comprising at least Ni on top of a SiGe containing substrate;

subjecting the structure to a self-aligned silicide process so as to form a solid solution of (Co, Ni) disilicide on said SiGe containing substrate, whereby said Ni reduces the formation temperature of the disilicide as compared to a Co layer not containing said Ni.

2. The method of Claim 1 wherein the self-aligned silicide process comprises a first anneal performed at a first temperature that is capable of forming a high resistance silicide phase material; a selective etch to remove unreacted metal from regions not in contact with the SiGe substrate; and a second anneal performed at a second temperature that is higher than the first temperature of the first anneal.

3. The method of Claim 2 wherein the first anneal is performed at a temperature of from about 400° to about 600°C for a time period from about 1 to about 90 seconds using a continuous heating regime or various ramp and soak heating cycles.

4. The method of Claim 2 wherein the second anneal is performed at a temperature of from about 600°C to about 800°C for a time period from about 1 to about 90 seconds using a continuous heating regime or various ramp and soak heating cycles.

5. The method of Claim 1 wherein the Co layer comprising at least Ni contains from about 0.1 to about 40 atomic percent Ni.

6. The method of Claim 5 wherein the Co layer comprising at least Ni contains from about 5 to about 30 atomic percent Ni.

7. The method of Claim 1 wherein the Co layer comprising at least Ni is a Co-Ni alloy or a multilayered stack comprised of Co/Ni or Ni/Co.

8. The method of Claim 1 wherein the Co layer comprising at least Ni further comprises an additive selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Cu, Y, Zr, Nb, Rh, In, Sn, La, Hf, Ta, W, Re, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, So, Er, Tm, Yb, Lu and mixtures thereof.

9. The method of Claim 8 wherein the additive is Ti, V, Cr, Zr, Nb, In, Sn, Hf, Ta, W, Re or Pt.

10. The method of Claim 8 wherein said additive is present in said Co layer comprising at least Ni in an amount of from about 0.1 to about 40 atomic percent.

11. The method of Claim 2 wherein said first and second anneals comprise a rapid thermal annealing (RTA) process.

12. The method of Claim 2 wherein said first and second anneals are each carried out in an inert, nitrogen or forming gas atmosphere.

13. The method of Claim 2 wherein the first and second anneals are each performed at a rate from about 25 to about 75°C/sec.

14. The method of Claim 1 wherein a diffusion barrier is formed atop the Co layer comprising at least Ni prior to said self-aligned silicide process.

15. The method of Claim 14 wherein the diffusion barrier comprises TiN, W, WN, or Ti.

16. The method of Claim 14 wherein the diffusion barrier is removed by a selective etching step of said self-aligned silicide process.

17. A method fabricating a silicide on the surface of a SiGe containing substrate comprising the steps of:

providing a structure including a Co layer comprising at least Ni on top of a SiGe containing substrate;

performing a first anneal at a first temperature that is capable of forming a high resistance silicide phase material by reacting said Co layer comprising Ni with Si present in said SiGe containing substrate;

selective etching the structure to remove unreacted metal from regions not in contact with the SiGe substrate; and

performing a second anneal at a second temperature that is higher than the first temperature of the first anneal, said second anneal converts the high resistance silicide phase material into a solid solution of (Co, Ni) disilicide, whereby said Ni reduces the formation temperature of the disilicide as compared to a Co layer not containing said Ni.

18. A semiconductor structure comprises:

a SiGe containing substrate; and

a solid solution of (Co, Ni) disilicide on said SiGe containing substrate.

19. The structure of Claim 18 wherein the SiGe containing substrate comprises a single crystalline material or a polycrystalline material.

20. The structure of Claim 18 wherein the SiGe containing substrate is selected from the group consisting of poly-SiGe, a SiGe alloy, SiGeC, a SiGe alloy-on-insulator, a SiGeC-on-insulator and Si-on-SiGe.

21. The structure of Claim 18 wherein said (Co, Ni) disilicide contains from about 0.03 to about 15 atomic percent Ni.

22. The structure of Claim 21 wherein said (Co, Ni) disilicide contains from about 2 to about 10 atomic percent Ni.

23. The structure of Claim 18 wherein said (Co, Ni) disilicide further comprises an additive selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Cu, Y, Zr, Nb, Rh, In, Sn, La, Hf, Ta, W, Re, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, So, Er, Tm, Yb, Lu and mixtures thereof.

24. The structure of Claim 23 wherein the additive is Ti, V, Cr, Zr, Nb, In, Sn, Hf, Ta, W, Re or Pt.

25. The structure of Claim 23 wherein the additive is present in the (Co, Ni) disilicide in an amount of from about 0.03 to about 15 atomic percent.

26. The structure of Claim 18 wherein the (Co, Ni) disilicide is located atop a single crystalline SiGe containing substrate, said single crystalline SiGe containing substrate including source/drain regions.

27. The structure of Claim 18 wherein the (Co, Ni) disilicide is formed atop a polycrystalline SiGe containing substrate, said polycrystalline SiGe containing substrate is formed atop a gate of a transistor.